(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 416 903 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 90309731.9

(51) Int. Cl.5: H01L 21/3205, H01L 23/525

(22) Date of filing: 05.09.90

(30) Priority: 07.09.89 US 404996
08.12.89 US 447969

(43) Date of publication of application:
13.03.91 Bulletin 91/11

(84) Designated Contracting States:
DE FR GB IT NL

(71) Applicant: PEER RESEARCH, Inc.
99 Tasman Drive, Suite 112
San Jose, California 95134(US)

(72) Inventor: Whitten, Ralph G.
5220 Sierra Road
San jose, California 95132(US)
Inventor: Bechtel, Richard L.
1376 Bluebird Court
Sunnyvale, California 94087(US)

Inventor: Thomas, Mammen
1081 Corvette Drive
San Jose, California 95129(US)
Inventor: Chua, Hua-Thye
12410 Barley Hills Road
Los Altos Hills, California 94022(US)
Inventor: Chan, Andrew K.
717 Gailen Avenue
Palo Alto, California 94303(US)
Inventor: Birkner, John M.
9 Valley Oak
Portola Valley, California 94025(US)

(74) Representative: Jones, Ian et al
W.P. THOMSON & CO. High Holborn House
52-54 High Holborn
London WC1V 6RY(GB)

(54) Method of fabricating a programmable interconnect structure.

(57) In one method for forming amorphous silicon antifuses with significantly reduced leakage current, a film of amorphous silicon is formed in a antifuse via between two electrodes. The amorphous silicon film is deposited using plasma enhanced chemical vapor deposition, preferably in an silane-argon environment and at a temperature between 200 and 500 degrees C, or reactively sputtered in a variety of reactive gases. In another method, an oxide layer is placed between two amorphous silicon film layers. In yet another method, one of the amorphous silicon film layers about the oxide layer is doped. In another embodiment, a layer of conductive, highly diffusible material is formed either on or under the amorphous silicon film. The feature size and thickness of the amorphous silicon film are selected to minimize further the leakage current while providing the desired programming voltage. A method also is described for for forming a field programmable gate array with antifuses.

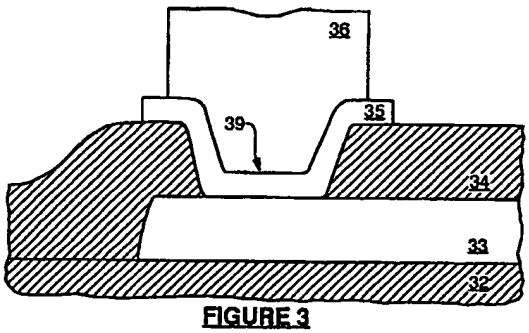


FIGURE 3

EP 0 416 903 A2

METHOD OF FABRICATING A PROGRAMMABLE INTERCONNECT STRUCTURE

The invention relates to a method of fabricating a programmable integrated circuit structure and to the programmable integrated circuit structures produced thereby.

Programmable semiconductor devices include programmable read only memories ("PROMs"), programmable logic devices ("PLDs"), and programmable gate arrays. Programmable elements suitable for one or more of these device types include fuses and antifuses.

A fuse is a structure which electrically couples a first terminal to a second terminal, but which, when programmed by passage of sufficient current between its terminals, electrically decouples the first terminal from the second terminal. A fuse typically is of a conductive material which has a geometry that causes portions of the conductive fuse material to physically separate from each other when heated to the extent that an open circuit results.

An antifuse is a structure which when unprogrammed does not electrically couple its first and second terminals, but which, when programmed by applying sufficient voltage between the first and second terminals, permanently electrically connects the first and second terminals. One type of antifuse comprises a high resistive material between two terminals of conductive material, the antifuse material being such that when sufficient voltage is applied, the resulting current heats the materials and causes portions of the conductive material to extend into the resistive material and form a permanent conductive path. Another type of antifuse comprises an amorphous silicon which forms conductive polysilicon when heated. In PROM devices, for example, the advantages of the antifuse technology over fuse technology include scalability and reduced programming current requirement. Various antifuses are disclosed in United States Patent No. 3,675,090, issued July 4, 1972 to Neale, and United States Patent No. 3,792,319, issued February 12, 1974 to Tsang.

The use of amorphous silicon in the fabrication of semiconductor threshold and switch devices is well known. As more fully discussed in the aforementioned Neale patent, various semiconductor switch devices comprise a "pore" filled with amorphous silicon, which contacts a lower electrode forming surface and an upper electrode forming surface. The electrodes are variously described as comprising a refractory material alone (Neale, Figure 4), a refractory material connected at its upper surface to an aluminum conductor (Neale, Figure 6), a refractory material overlaying an aluminum conductor (Neale, Figures 8-9), and a refractory material connected at its end to an aluminum conductor (Neale, Figure 11).

Neale recognized that two important objectives were to obtain switch devices with a very low leakage current in the preprogrammed condition and a fairly consistent programming voltage value. An aspect of the Neale invention was to fabricate the semiconductor switch device so as to present a very small cross-sectional area of semiconductor material for current flow to minimize leakage current paths therethrough. Unfortunately, these measures alone are insufficient to achieve low leakage current along with a low and consistent programming voltage, which is desired in many applications.

Antifuses have been used successfully in programmable interconnect substrates, memories, and some types of PLDs.

An antifuse suitable for use in an electrically programmable interconnection substrate is disclosed in US Patent No. 4,458,297, issued July 3, 1984 to Stopper et al. A silicon substrate for hybrid circuits is divided into discrete areas for hosting integrated circuit chips and providing the bonding pads for the signal connections between the chips and the substrate. Transverse pad lines and net lines are provided, which are insulated at the crossover points except for respective via holes, each furnished with a pad of amorphous silicon material. The lines are arranged so that a number of pads can be connected to each other as desired by programming. See also Herbert Stopper, "A Wafer with Electrically Programmable Interconnections," in Proceedings of the International Solid State Circuits Conference, February 15, 1985, pp. 263-269.

Antifuses used in interconnect substrates tend to require high programming voltages and currents. As the interconnection substrate does not contain sensitive integrated active semiconductor devices, and as programming is completed prior to attachment and bonding of the functional die, the antifuses between the pad and net lines are designed to minimize the leakage current, and do not minimize the programming current and programming voltage.

Specifically the device described by Stopper requires that a threshold voltage of 20 volts be exceeded to initiate the switching process into the programmed state. Many devices designed to operate at 5 volts (the typical integrated circuit operating voltage) cannot tolerate voltages as high as 20 volts due to junction breakdown voltages between 12-20 volts. Although higher junction breakdown voltages can be obtained in integrated circuits, thicker insulation layers throughout the cir-

cuit, larger transistors, lower doping levels, and other component adjustments must be provided. These changes cause a reduction in the operating frequency as well as an increase in the size of the circuit. Thus a higher breakdown voltage is accompanied by a direct trade-off in circuit performance.

An example of antifuse technology for a bipolar PROM is illustrated in Figures 1 and 2 of the accompanying drawings which are taken from Brian Cook and Steve Keller, "Amorphous Silicon Antifuse Technology for Bipolar PROMs," 1986 Bipolar Circuits and Technology Meeting, 1986, pp.99-100, and are cross-sectional illustrations of prior art amorphous silicon antifuse structures.

In the via antifuse of Figure 1, first metal comprising aluminum conductor 14 and barrier metal 10 and 11 is provided on an oxide layer 13 overlaying substrate 12. A thick oxide layer 18 is provided over conductor 14 as insulation from second metal. A via etched into oxide layer 18 is lined with a thin film of amorphous silicon 15, which fully overlays and contacts the barrier metal 11 under the via. Second metal comprising barrier metal 16 and aluminum conductor 17 is provided over the via, in contact with the amorphous silicon 15.

The contact antifuse of Figure 2 is formed over a transistor comprising collector 20, base 21, and emitter 22. Emitter contact is made to a platinum silicide region 23 through a contact hole in oxide 24, which is lined with amorphous silicon film 25. Barrier metal 26 and aluminum conductor 27 overlay the amorphous silicon 25, and are protected by oxide 28.

In the examples of Figures 1 and 2, the deposition of the amorphous silicon was a critical step in the process, as the thickness of the film 15 (Figure 1) and film 25 (Figure 2) was thought to control the programming voltage. The pre-programmed leakage current was reduced to about 6 microamperes at 2 volts by a high temperature anneal at 450 degrees C. Other factors thought to influence leakage current in the undoped amorphous silicon antifuse were feature size (leakage current proportional) and film thickness (leakage current inversely proportional).

Unfortunately, antifuse technology developed for use in memories is generally too leaky for use in PLDs, as noted by Cook et al. In a PROM, one bit is selected per output at a time; therefore, if the programmable elements are leaky, only one leaky bit loads the sense amplifier. Usually the sense amplifier can tolerate this loading without drastically affecting its functionality or performance. Contrast one type of PLD known as a programmable array logic, which is implemented using PROM technology. The programmable elements are used to configure logic (routing is dedicated and global). In programmable array logic, multiple bits can be accessed and may overload the sense line if the programmable elements are leaky. Overloading the sense line may drastically degrade the performance and in the extreme case, result in functional failure.

Certain techniques have been employed in PLDs using antifuse technology to overcome the problems created by antifuse leakage. One technique uses active semiconductor devices such as diodes or transistors to block the leakage current, an approach which can also be used in memories having leaky antifuses. While this approach is satisfactory in memories and in the logic configuration circuits of PLDs, the technique is not satisfactory for use in the routing circuits of such integrated circuits as the field programmable gate array ("FPGA").

The FPGA, which is distinguished from conventional gate arrays by being user programmable, otherwise resembles a conventional gate array in having an interior matrix of logic blocks and a surrounding ring of I/O interface blocks. Logic functions, I/O functions, and routing of interconnect networks are all user configurable, which affords high density and enormous flexibility suitable for most logic designs. User logic, for example, conventionally is implemented by interconnecting two-input NAND gates into more complex functions. Extensive user configurability of the FPGA is achieved by incorporating a large number of programmable elements into the logic and I/O blocks and the interconnect network. Naturally, the leakage requirement of the programmable elements is stringent, due to the large number of possible connections generally involved and the numerous failure modes that leakage can cause. For instance, leaky programmable elements in the routing areas contribute to high supply current problems, cross talk problems, and performance degradation.

To meet the stringent leakage requirements imposed by FPGAs, conventional fuses and transistor switches generally have been employed. Antifuses using amorphous silicon have not been employed due to their excessive leakage when designed for the programming voltages and currents conventionally used in FPGAs.

In accordance with the present invention, some embodiments of amorphous silicon antifuses offer a low leakage current while requiring programming voltages, currents, and time compatible with such devices as field programmable gate arrays.

Some embodiments of the amorphous silicon antifuses of the present invention combine an operating voltage of 5 to 5.5 volts with a programming voltage above 10 volts but under 20 volts.

These and other advantages are achieved in the present invention, a method for fabricating a programmable interconnect structure for an inte-

grated circuit. The method generally includes the steps of fabricating a first conductor; fabricating an insulating layer overlaying the first conductor; fabricating an opening through the insulating layer at a selected location and terminating the opening at a portion of the first conductor; forming a layer of an antifuse material; patterning the antifuse material to form at the selected location an antifuse feature substantially restricted to the opening, the feature having a region contacting and fully overlaying the first conductor portion; and fabricating a second conductor, wherein a portion of the second conductor contacts and overlays the amorphous silicon region. In one embodiment, the antifuse material is amorphous silicon, deposited using either plasma enhanced chemical vapor deposition or reactive ion sputtering. In another embodiment, the antifuse material includes a layer of a conductive, highly diffusible material formed either on or under the amorphous silicon film. In yet another embodiment of the present invention, the antifuse material includes a dielectric layer formed between two layers of amorphous silicon film. In a variation of this embodiment, one of the silicon layers is doped.

The invention is further described below, by way of example, with reference to the remaining figures of the accompanying drawings, in which:

Figures 3-7 are cross-sectional illustrations of specific features of various embodiments of the present invention;

Figures 8A & 8B are a cross-section illustration of a completed programmable CMOS integrated circuit having amorphous silicon antifuses in accordance with the present invention; and

Figure 9 is a graph illustrating current voltage characteristics of an antifuse fabricated in accordance with the present invention.

In the drawings, like reference numerals indicate like parts.

Several embodiments of antifuses suitable for use in, for example, the semiconductor structure of Figure 7 are illustrated in Figures 3-6. Considerations particular to each of the embodiments are described below, followed by a description of the semiconductor structure.

The antifuses illustrated in Figures 3-6 include a semiconductive substrate (not shown), a dielectric layer 32, a first conductive layer 33, a second conductive layer 36, a dielectric layer 34 including via 39, and an amorphous silicon structure 35 extending into via 39 and contacting both the first conductive layer 33 and the second conductive layer 36. The first dielectric layer 32, typically silicon dioxide, is patterned to expose substrate 31, typically silicon, at locations where portions of first conductive layer 33, typically polycrystalline silicon or aluminum, contact substrate 31. Likewise vias such as via 39 are formed in second dielectric 34, also typically silicon dioxide, where first conductive layer 33 is to be exposed. Antifuses may be formed in some such vias of the integrated circuit and not in other vias.

The following basic steps are used in the process for forming an antifuse of this invention. A layer of dielectric 32, typically silicon dioxide, is formed on the silicon substrate, and patterned to expose portions of the substrate 31. Alternatively, the dielectric layer 32 may be formed upon a lower conductive layer (not shown) rather than to substrate 31. A first conductive layer 33 of, for example, aluminum or polycrystalline silicon, is formed on the dielectric 32. First conductive layer 33 is patterned to form appropriate interconnects. A second layer of dielectric 34, again typically silicon dioxide, is formed on the first conductive layer 33 and patterned to form vias such as via 39 exposing first conductive layer 33. Some of these vias, in particular via 39, will serve as sites for antifuses. Other vias, not shown, may allow for direct connection between first conductive layer 33 and a to-be-formed second conductive layer 36.

Into those vias which will have antifuses is formed the antifuse structure 35, as will be discussed. The antifuse material may extend somewhat beyond the edge of the via 39 which it fills. Next, second conductive layer 36, typically a metal such as aluminum, is applied and patterned, followed by application and patterning of a final passivation layer (not shown), typically a silicon oxide or silicon nitride.

Generally, the antifuses of Figures 3-6 are particularly advantageous for applications which require that the antifuse reliably does not program at a voltage below 7.5 volts and reliably programs at a voltage above 10 volts. The range between 7.5 volts and 10 volts is a guard band. Such applications also require that the antifuses pass very little current until programmed; leakage across the antifuses prior to programming of less than 10 nanoamperes at 5.5 volts is desirable.

The four illustrative antifuse structures illustrated in Figures 3-7 are now described.

The antifuse structure 35 shown in Figure 3 is a layer of amorphous silicon film. At this point, several process and structural parameters can be identified as important, especially for amorphous silicon antifuses designed for use in FPGAs and other integrated circuit applications sensitive to leakage current. These parameters influence important characteristics of the antifuse, including trigger current (current at initiation of the programming mechanism), programming voltage (voltage at initiation of the programming mechanism), programming current (current provided to form electrical connection upon which the programmed resistance

depends), programming time (period over which the programming current is maintained), leakage current, and reproducibility of the structure (necessary to maintain high yield).

The programming voltage is controlled by the thickness of the amorphous silicon film 35 in contact with the conductor 33 at the bottom of the antifuse via 39. Film 35 is deposited to a thickness of about 2000 Angstroms, which results in a programming voltage of about 12 volts. Of course, other programming voltages may be achieved by depositing film 35 to an appropriate thickness. The leakage current is controlled by several factors, including feature size and film thickness. Feature size and film thickness are selected to minimize leakage current, consistent with the process used and the programming voltage desired. In the present embodiment, the feature size is about 1.5 um and, as has been mentioned, the film thickness is 2000 Angstroms.

We have found that another factor controlling leakage current is the manner of deposition of the amorphous silicon film. In one embodiment, the amorphous silicon film 35 is deposited using plasma enhanced chemical vapor deposition ("PECVD"), rather than CVD or LPCVD. The reaction chamber used was a model GL560, manufactured by Pacific Western Systems of Mountain View, California. The process reactants were SiH4 and argon. Certain reactive gases including oxygen, hydrogen, nitrogen, fluorine, and chlorine can be added to the basic process reactants. These reactive gases act as like dopants to modify the electrical characteristics and reduce the conductivity of the amorphous silicon. The process parameters are selected so that dopant concentration in the film is in the range of 0 to 30 atomic percent. The reaction was carried out at a temperature of 225 degrees C, although it is believed that 380 degrees C could be advantageously used. In fact, temperatures within the range of about 200 degrees C to about 500 degrees C are believed suitable. The resultant deposition and evolved by-products were amorphous silicon and hydrogen.

Amorphous silicon formation by plasma enhanced chemical vapor deposition (PECVD) is described generally in A.C. Adams, "Plasma Deposition of Inorganic Films," Solid State Technology, April 1983, p. 135, hereby incorporated herein by reference thereto.

In another embodiment, the amorphous silicon film 35 is deposited using reactive sputter deposition. Preferably, the amorphous silicon material 35 is deposited in one or more of the following reactive gases: oxygen, hydrogen, nitrogen, fluorine, chlorine, or argon. Amorphous silicon formation by sputter deposition is described generally in D.L. Morel and T.D. Moustakas, "Effect of hydrogen on the diode properties of reactively sputtered amorphous silicon Schottky barrier structures," Applied Physics Letters, Vol. 39, No. 8, October 15, 1981, pp. 612-14, hereby incorporated herein by reference thereto.

Both PECVD and reactive sputtering enables the formation of a amorphous silicon film having, it is believed, small randomly oriented silicon crystals. In the case of PECVD, the character of the silicon crystals is achieved by the low temperature at which the amorphous silicon is deposited. In the case of sputter deposition as well as PECVD, the small randomly ordered character of the silicon crystals is enhanced by the interaction of reactive gases with the silicon species during deposition. These dopants tie-up dangling molecular bonds and form interstructural compounds that deter recrystallization of the amorphous silicon, thus minimizing the current leakage through the unprogrammed antifuse 35 between first and second conductive layers 33 and 36. To preserve the special character of the amorphous silicon layer 35 deposited using the PECVD or sputter deposition technique, care should be taken during subsequent processing steps to avoid sustained high temperature operations.

In both deposition techniques, the dopant incorporation into layer 35 is obtained by introducing a partial pressure of the desired dopant gas to the deposition system in which the device is being fabricated. The gases listed above are chosen specifically to reduce the conductivity of the amorphous silicon. Alternatively or additionally, doping may also be accomplished by other techniques, such as by ion implantation after deposition of antifuse material 35, followed by a rapid thermal anneal. A suitable machine for performing the rapid thermal anneal is the Heatpulse (Trademark) model 2106, available from AG Associates of Sunnyvale, California.

Dopant concentration is determined as follows. The lower limit of the dopant concentration is determined by the allowable leakage current of the link. The upper limit is determined by two key changes in the physical properties; namely, increased programming voltage and increased programming current. Increased programming voltage is due to increased dielectric strength of the antifuse material, and increased programming current is due to the increased difficulty of forming an alloy, conductive filament, or metallic compound, as the case may be. In the case in which layers 33 and 36 are aluminum and layer 35 is silicon, the increase in programming voltage and current is due to the increased difficulty of forming an Al-Si eutectic through the antifuse which provides the low resistance after programming.

By careful control of feature size, film thick-

ness, and manner of deposition of the amorphous silicon, an amorphous silicon antifuse with low programming voltage and low leakage current is achieved. The deposition technique described herein may be combined with various feature sizes and film thicknesses to achieve other programming voltages, while preserving a low leakage current.

In the embodiment of Figure 4, antifuse layer 40 comprises three layers of material, the middle layer 45 being a thin layer of dielectric. The thin dielectric layer 45 is effective in reducing the leakage current before programming without significantly increasing the required programming voltage. An oxide layer 45 only 10-20 angstroms thick can achieve this purpose. First layer 44 of antifuse layer 40 is of one of the materials described in the embodiment of Figure 3 for forming antifuse layer 35. In the embodiment of Figure 4, polycrystalline silicon may also be used to form layer 44. Next, thin dielectric layer 45 is formed, preferably by oxidizing the exposed polycrystalline silicon of layer 44. An effective process for producing a uniform thin oxide layer 45 is to oxidize polycrystalline silicon layer 44 at a low temperature such as, for example, 350-450 degrees C in a standard oxidation furnace. Alternatively, or additionally, the oxidation can be achieved by subjecting layer 44 to concentrated nitric acid (70% by volume aqueous solution) at 120 degrees C. This and other oxidizing agents such as sulphuric acid and hydrogen peroxide, or oxidizing procedures such as described by Werner Kern in "Purifying Si and SiO2 Surfaces with Hydrogen Peroxide," Semiconductor International, p. 94, April 1984, may be used for producing a nonporous oxide layer 45. The thickness of oxide layer 45 is self-limiting because as layer 44 becomes covered, there is no more surface material available to be oxidized and insufficient energy for species diffusion oxidation. Layer 45 seals the surface of layer 44 everywhere layer 44 is exposed to nitric acid. Subsequently a second layer 46 of doped or undoped PECVD amorphous silicon, polycrystalline silicon or reactive sputtered silicon is formed. All three layers are patterned in the same masking step.

In the embodiment of Figure 5, a layer 55 of silicon material having one of the compositions, doped or undoped PECVD amorphous or reactive sputtered silicon, described with respect to layer 35 of the embodiment of Figure 3, and a thin layer 56 of a conductive, highly diffusible material such as aluminum, gold, copper, or boron (from a layer of boron nitride). The layer 56 is formed in the same masking step as the patterned layer 55, or alternatively, may be formed in the second metal masking step. Layer 56 serves as a source of conductive material (aluminum, gold, copper, or boron) for forming a conductive path 57 (see Figure 5b) during the programming process. Layer 56 must be sufficiently thick to provide adequate conductive material, and have the property of being stable at low temperatures but highly susceptible to diffusion above 400 degrees C. A layer 500-2000 Angstroms thick is generally sufficient for metals, while a layer 20-200 Angstroms thick is generally sufficient for boron nitride. As shown in Figure 6, when a programming voltage is applied between conductive layers 33 and 36, dielectric layer 55 will be punctured along a path 57 of least resistance. Electrons flowing along this path will cause local heating. In the presence of such heating, the material in layer 56 will diffuse rapidly along path 57, forming a highly conductive alloy with silicon material of layer 55 along path 57, and providing a permanent connection between conductive layers 33 and 36 after the programming voltage is removed.

In the embodiment of Figure 7, a three-layer antifuse layer 60 comprises a low-conductivity layer 64 of undoped PECVD amorphous silicon, undoped polycrystalline silicon, or undoped reactive sputtered amorphous silicon, adjacent to dielectric 65, which comprises a thin oxide layer similar to layer 45 of the Figure 4 embodiment. Layer 65 is adjacent to a doped polysilicon layer 66. Layer 66 may be doped with any of the standard silicon dopants such as arsenic, boron, or phosphorus, or with any of the fast diffusing materials such as gold or copper. Layer 66 functions in a manner similar to layer 56 of the embodiment of Figures 5 and 6, providing a source of conductive ions to form a path through layers 65 and 64. If the combined thickness of layers 64, 65, and 66 is the same as the thickness of layer 35 of the Figure 3 embodiment, then thin dielectric layer 65 may need to be made thicker in order to reduce pre-programming leakage current to an acceptable level. In addition, even if layers 64 and 66 were made thicker, so that layer 65 was not needed for reducing leakage current, layer 65 would under a certain circumstances be desirable in order to prevent the dopants in layer 66 from diffusing into layer 64 during manufacture. All three layers 64, 65 and 66 are patterned in the same masking step.

The particular embodiments shown in Figures 3-7 are suitable for use in an integrated circuit having an operating voltage of 5 to 5.5 volts. The various antifuse embodiments have the ability to withstand, that is, to resist programming at an operating voltage up to 7.5 volts. As an integrated circuit generally has the ability to withstand voltages of up to 15 volts, the various antifuse embodiments are suitable for programming within a range of 10-15 volts, 12 volts being preferred for a safe operating margin. Other embodiments having other operating and programming voltages can be

fabricated according to the principles described herein. For example, an antifuse for circuit operating at 2 volts may be manufactured to program at 6 volts. For amorphous silicon, programming voltage is approximately proportional to the square root of the thickness of the antifuse material across which the voltage is applied.

Various other embodiments, which are not illustrated, include the following. In one variation, an antifuse layer comprises a layer of diffusible material such as the aluminum, gold, copper or boron nitride (a source for boron), similar to layer 56 of the Figure 5 embodiment, is added to the three-part antifuse layer 40 of Figure 4. Another variation comprises a layer of diffusible highly conductive material such as aluminum, gold, copper or boron (from a layer of boron nitride), similar to layer 56 of the Figure 5 embodiment, substituted for the doped silicon layer 66 of the Figure 7 embodiment. Other variations are obtained by altering the orientation of the layers shown in Figures 3-7. For example, layers 64 and 66 of Figure 7 can be reversed. In another variation, layers 55 and 56 of Figure 5 are reversed, and layer 56 is formed on first metal layer 33 before deposition of dielectric layer 55.

A cross sectional view of a CMOS programmable gate array structure having antifuses in accordance with the Figure 3 embodiment of the present invention is illustrated in Figure 8. Suitable CMOS processes are well known and commercially available, and the particular CMOS structure shown is exemplary. The present invention is applicable to integrated circuit structures of any type formed by any process, whether memory, logic, digital or analog, and including NMOS, PMOS, Bipolar, BICMOS, Gallium Arsenide, and others.

Substrate 100 is provided with an N-well 102 and P-doped substrate region 104. A PMOS device 160 comprises source and drain regions 106 and 108 and gate 110. A first NMOS device 162 comprises source and drain regions 112 and 114, and gate 116. A second NMOS device 164 comprising source and drain regions 113 and 115 and gate 117 also is present.

Patterned oxide layers 118 and 120 (shown in crosshatch) also are present. As is well known in the art, oxide layer 118 comprises various oxide layers (not shown) including a field oxide, while oxide layer 120 comprises various oxide layers (not shown) formed in the fabrication of gates 110, 116, and 117. The oxide layers 118 and 120 are suitably patterned and etched to form contact holes down to the various source and drain regions 106, 108, 112, 114, 113 and 115.

Using standard techniques, a thin film 122 of TiW measuring about 2500 Angstroms is sputtered over the patterned oxide layers and into the contact holes to regions 106, 108, 112, 114, 113 and 115. Other suitable barrier metals may be used instead of TiW, and the TiW may be combined with other layers such as, for example, platinum silicide at the source and drain regions, as is well known in the art. Using standard techniques, a film 124 of aluminum measuring about 6000 Angstroms is sputtered over the TiW film 122. Other metals may be used as well, as is well known in the art.

First metal lines are formed as follows. The aluminum film 124 is patterned and etched using a BCl3, Cl2, CHCl3 standard aluminum dry etch. Using the remaining aluminum as a mask, the TiW film 122 is RIE etched using CHF3 and 02. A metal opening mask is used to pattern openings in the first metal lines, which serve as sites for formation of antifuses 156 and 158. The portions of the aluminum layer 124 remaining after the first aluminum etch is patterned and again etched using a BCl3, Cl2, CHCl3 standard aluminum dry itch down to the TiW layer 122.

The second interlevel dielectric is a thick oxide layer 132 of about 9000 Angstroms thickness, deposited using any suitable standard technique such as, for example, plasma enhanced chemical vapor deposition. In one of many suitable techniques, the layer 132 comprises two oxide layers (not shown). The first oxide layer is deposited to a selected thickness and planarized. The planarization step involves spinning a resist layer over the deposited oxide and reflowing the resist with a postbake, after which the surface is planarized in an RIE etch-back adjusted for equal resist and oxide etch rates. A second oxide layer then is deposited to ensure dielectric integrity and a 9000 Angstrom thickness over the irregular topography.

Antifuse vias are now formed through the oxide 132 down to the TiW layer 122. An antifuse via mask similar to the metal opening mask but having smaller via dimensions is used to pattern the oxide, and vias are etched to the TiW layer 122 using standard RIE techniques.

The amorphous silicon material is deposited in the next process step. A thin film 142 of amorphous silicon is deposited over oxide layer 132, and conforms to the topography of the oxide layer 132 and the vias made therein. The layer 142 is patterned and etched to remove amorphous silicon except in the antifuse vias, as shown. Preferably, the amorphous silicon material is deposited using PECVD, as described with respect to Figure 3 above, although sputter deposition as described with respect to Figure 3 above is suitable as well. Moreover, any of the various antifuse layers discussed herein may be used as well, together with appropriate modifications to the first and second metal systems.

When the Figure 3 embodiment is used in an integrated circuit, reproducibility is improved by

eliminating aluminum in the conductor underlying the amorphous silicon film. It has been found that the top surface of aluminum conductors such as conductor 124 tend to have an irregular topography when compared with the thickness selected for the amorphous silicon film 142. The irregular topography causes non-uniform antifuse characteristics and shorts. To avoid the problem, the amorphous silicon material is deposited in a via etched down to a thin film refractory metal such as the TiW layer 122, which is deposited on a planarized regular surface such as the oxide 118. Of course, other metal films may be used as well, provided they can be deposited or otherwise processed to present a smooth topography relative to the thickness of the amorphous silicon film 142.

Processing proceeds with the sputter deposition of a thin film 144 of TiW of about 1000 Angstroms, followed by a sputter deposition of an aluminum film 146 of about 1.0 um. The films 144 and 146 are patterned and etched substantially as described above, resulting in the second metal interconnect. The resulting structure is passivated (layer 148) using any suitable technique, such as PECVD of deposition of SiO2.

Completed antifuses 156 and 158 are illustrated in Figure 8, where they can be programmed to connect NMOS device 162 to second metal interconnect 146, or to connect NMOS device 164 to second metal interconnect 146, or to connect NMOS device 162 to NMOS device 164. Such a programmable element might occur between devices within a circuit block, or in a routing system connecting circuit block to circuit block, or in an interconnect system as between third and fourth metal.

The characteristics of an experimental antifuse fabricated by an PECVD process as described with respect to Figure 3 is illustrated in Figure 8, which is a current-voltage plot. The preprogramming leakage current at 5.5 volts was 7.6 nA. The programming voltage was 10.6 volts, and the trigger current was 10.9 uA. Generally, PECVD antifuses fabricated as set forth herein have a leakage current of under 10 nanoamperes at 5.5 volts and have a programmed resistance of under 200 ohms, for a programming voltage of about 12 volts, a programming current of 5 mA, and a programming time of 1 msec. Such antifuses are satisfactory for use in such devices as FPGAs. By varying the design, such as providing an aluminum-only metal system about the amorphous silicon antifuse, and by varying other parameters, such as increasing the programming current to 50 mA, a programmed resistance of as little as 9 ohms can be achieved.

While our invention has been described with respect to the embodiments included above, other embodiments and variations not described herein may be considered to be within the scope of our invention. For example, our invention should not be limited by the composition of the metal system used for the interconnects, or to any specific thickness of the various films and oxides used in the structure. These other embodiments and variations are to be considered within the scope of our invention, as defined by the following claims.

Claims

1. A method of fabricating a programmable interconnect structure for an integrated circuit having a plurality of devices, comprising the steps of:
fabricating a first conductor (33);
fabricating an insulating layer (34) overlaying the first conductor;
fabricating an opening through the insulating layer at a selected location and terminating the opening at a portion of the first conductor;
depositing using plasma enhanced chemical vapor deposition a film (35) of amorphous silicon upon the insulating layer and in the opening;
patterning the amorphous silicon film to form at the selected location an amorphous silicon feature substantially restricted to the opening and having a region contacting nd fully overlaying the first conductor portion; and
fabricating a second conductor (36) of which a portion contacts and overlays the amorphous silicon region.

2. A method as claimed in claim 1 wherein plasma enhanced chemical vapor deposition proceeds at a temperature selected from the range 200 degrees C to 500 degrees C.

3. A method as claimed in claim 1 wherein the amorphous silicon depositing step comprises the step of establishing a reaction condition of argon at 225 degrees C, 340 degrees C or 380 degrees C.

4. A method of fabricating a programmable interconnect structure for an integrated circuit having a plurality of devices, comprising the steps of:
fabricating a first conductor (33);
fabricating an insulating layer (34) overlaying the first conductor;
fabricating an opening through the insulating layer at a selected location and terminating the opening at a portion of the first conductor;
depositing using reactive sputter deposition a film (35) of amorphous silicon upon the insulating layer and in the opening;
patterning the amorphous silicon film to form at the selected location an amorphous silicon feature substantially restricted to the opening and having a region contacting and fully overlaying the first conductor portion; and
fabricating a second conductor (36) of which a

portion contacts and overlays the amorphous silicon region.

5. A method as claimed in claim 1 or 4 wherein the depositing step comprises depositing the amorphous silicon film in a reactive gas atmosphere comprising argon, oxygen, hydrogen, nitrogen, fluorine, or chlorine.

6. A method as claimed in claim 1 or 4 comprising the step of ion implanting a dopant in the amorphous silicon film following the amorphous silicon depositing step.

7. A method as claimed in claim 6 wherein the dopant comprises argon, oxygen, hydrogen, nitrogen, fluorine, or chlorine.

8. A method as claimed in any preceding claim wherein the first conductor fabricating step comprises the step of forming a refractory metal surface on the first conductor portion.

9. A method as claimed in any preceding claim wherein the second conductor fabricating step comprises the step of forming a refractory metal surface on the second conductor portion.

10. A method of fabricating a field programmable gate array, comprising the steps of:

forming logic circuits for performing logic functions;

forming I/O circuits for performing I/O functions;

forming a first level of conductive routing channels (122,124) connected to select input and output terminals of the logic and I/O circuits;

forming an insulating layer (34;132) overlaying the first level routing channels;

forming openings through the insulating layer at selected locations and terminating the openings upon selected channels of the first level routing channels;

blanket depositing using plasma enhanced chemical vapor deposition a film (35;142) of amorphous silicon upon the insulating layer, wherein the film is within the openings and contacts and fully overlays the first level channels at the select locations;

patterning the amorphous silicon film to form at the selected locations respective amorphous silicon film areas substantially restricted to the openings; and

forming a second level of conductive routing channels (144,146), the second level channels being connected to select input and output terminals of the logic and I/O circuits, and being transverse to the first level channels and in contact with and overlaying the film areas at the selected locations.

11. A method of fabricating a field programmable gate array, comprising the steps of:

forming logic circuits for performing logic functions;

forming I/O circuits for performing I/O functions;

forming a first level of conductive routing channels (122,124) connected to select input and output terminals of the logic and I/O circuits;

forming an insulating layer (34;132) overlaying the first level routing channels;

forming openings through the insulating layer at selected locations and terminating the openings upon selected channels of the first level routing channels;

blanket depositing using reactive sputter deposition a film (35;142) of amorphous silicon upon the insulating layer, wherein the film is within the openings and contacts and fully overlays the first level channels at the select locations;

patterning the amorphous silicon film to form at the selected locations respective amorphous silicon film areas substantially restricted to the openings; and

forming a second level of conductive routing channels, the second level channels being connected to select input and output terminals of the logic and I/O circuits, and being transverse to the first level channels and in contact with and overlaying the film areas at the selected locations.

12. A method as claimed in claim 10 or 11 wherein:

the first level forming step comprises the step of forming selected ones of the first level channels in a plurality of discrete segments;

the opening forming step comprises the step of forming openings through the insulating layer at selected locations proximate the opposing ends of the discrete segments, and terminating the openings upon the discrete segments;

the patterning step comprises the step of patterning the amorphous silicon film to form, with respect to each pair of openings to adjacent channel segments, at least one amorphous silicon film area; and

the second level forming step comprises the step of forming, with respect to each pair of openings to adjacent channel segments, a conductive segment in contact with and overlaying the film area associated therewith.

13. A method of fabricating a programmable interconnect structure for an integrated circuit having a plurality of devices, comprising the steps of:

fabricating a first conductor (33);

fabricating an insulating layer (34) overlaying the first conductor;

fabricating an opening through the insulating layer at a selected location and terminating the opening at a portion of said first conductor;

depositing a first film (44;64) of amorphous or polycrystalline silicon upon the insulating layer and in the opening;

forming a dielectric layer (45;65) on the first film;

depositing a second film (46;66) of amorphous or polycrystalline silicon upon the dielectric layer;

patterning the first and second films and the dielectric layer to form at the selected location an anti fuse feature substantially restricted to the opening and having a region contacting and fully overlaying

the first conductor portion; and
fabricating a second conductor (36) of which a portion contacts and overlays the antifuse feature region.

14. A method as claimed in claim 13 wherein the dielectric layer forming step comprises th step of growing a thermal oxide on the first film with rapid thermal anneal.

15. A method as claimed in claim 13 wherein the dielectric layer forming step comprises the step of exposing the first film to an oxidizing agent.

16. A method as claimed in claim 13, 14 or 15 comprising the step of doping the first film

17. A method as claimed in claim 13, 14, 15 or 16 comprising the step of doping the second film.

18. A method of fabricating a programmable interconnect structure for an integrated circuit having a plurality of devices, comprising the steps of:
fabricating a first conductor (33);
fabricating an insulating layer (34) overlaying the first conductor;
fabricating an opening through the insulating layer at a selected location and terminating the opening at a portion of the first conductor;
depositing a film (55) of amorphous silicon upon the insulating layer and in the opening;
forming a layer (56) of a conductive, highly diffusible material on the film;
patterning the film and the diffusible layer to form at the selected location an antifuse feature substantially restricted to the opening, the feature having a region contacting and fully overlaying the first conductor portion; and
fabricating a second conductor (36) of which a portion contacts and overlays the antifuse feature region.

19. A method of fabricating a programmable interconnect structure for an integrated circuit having a plurality of devices, comprising the steps of:
fabricating a first conductor;
fabricating an insulating layer overlaying the first conductor;
fabricating an opening through the insulating layer at a selected location and terminating the opening at a portion of said first conductor;
forming a layer of a conductive, highly diffusible material in the opening;
depositing a film of amorphous silicon upon the diffusible layer;
patterning the film and the diffusible layer to form at the selected location an antifuse feature substantially restricted to the opening and having a region contacting and fully overlaying the first conductor portion; and
fabricating a second conductor of which a portion contacts and overlays the antifuse feature region.

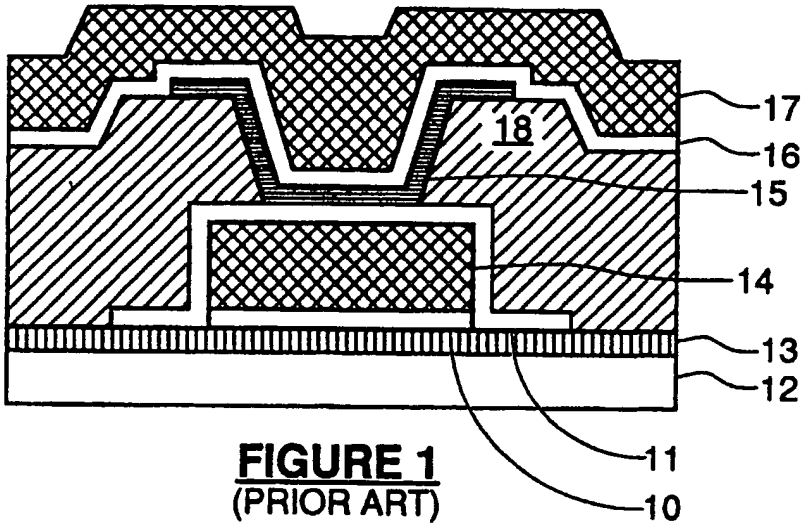
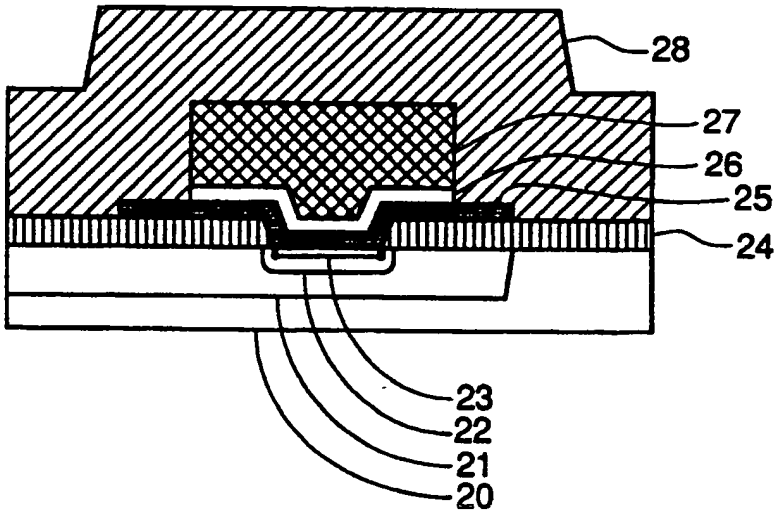


FIGURE 1
(PRIOR ART)

FIGURE 2
(PRIOR ART)



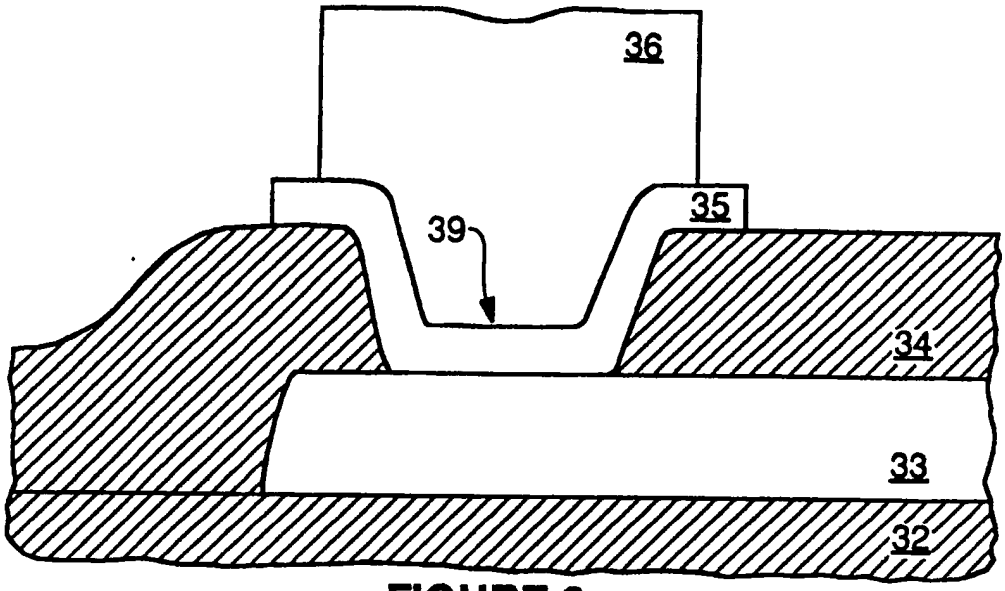


FIGURE 3

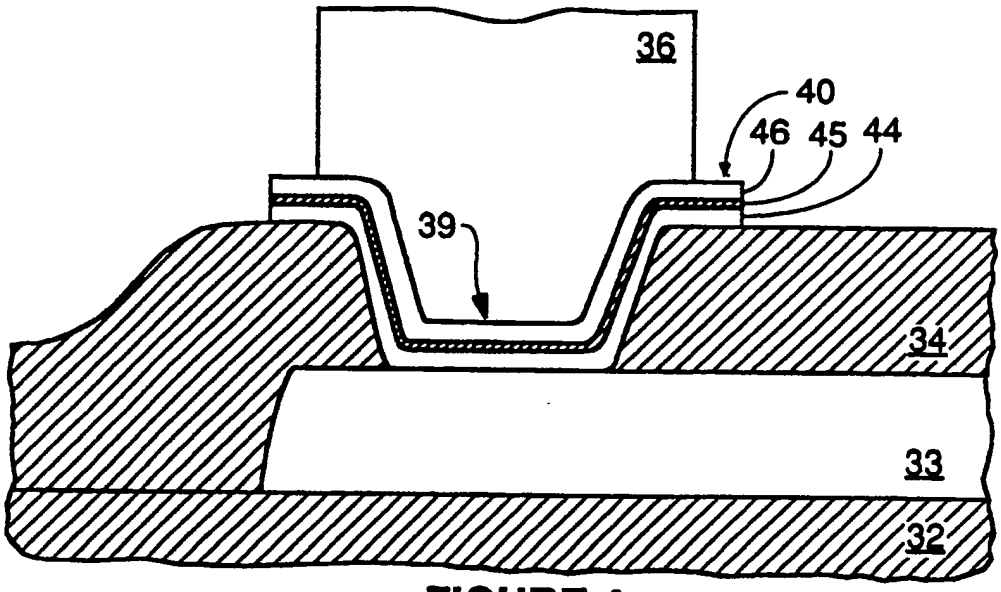


FIGURE 4

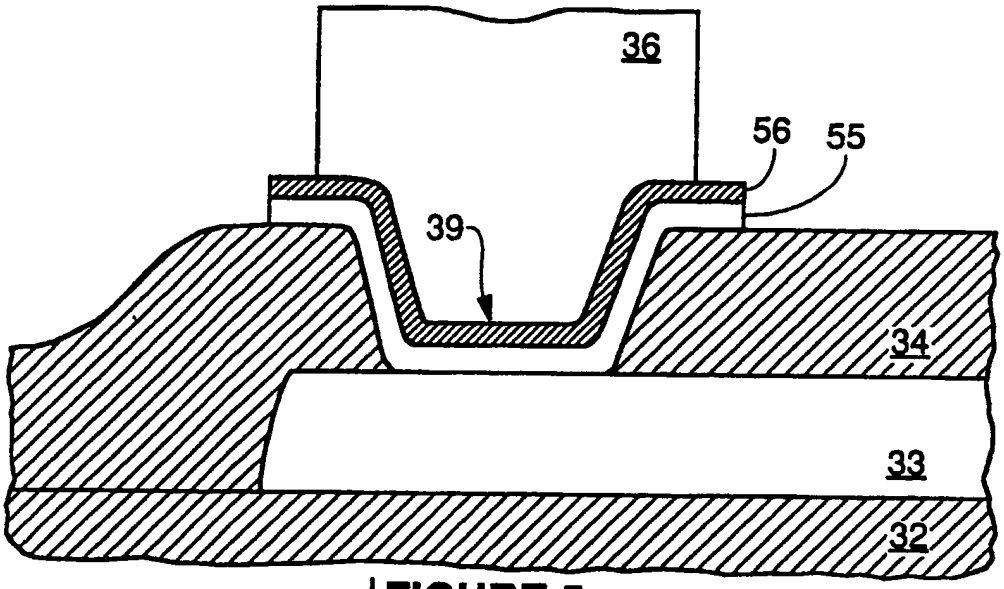


FIGURE 5

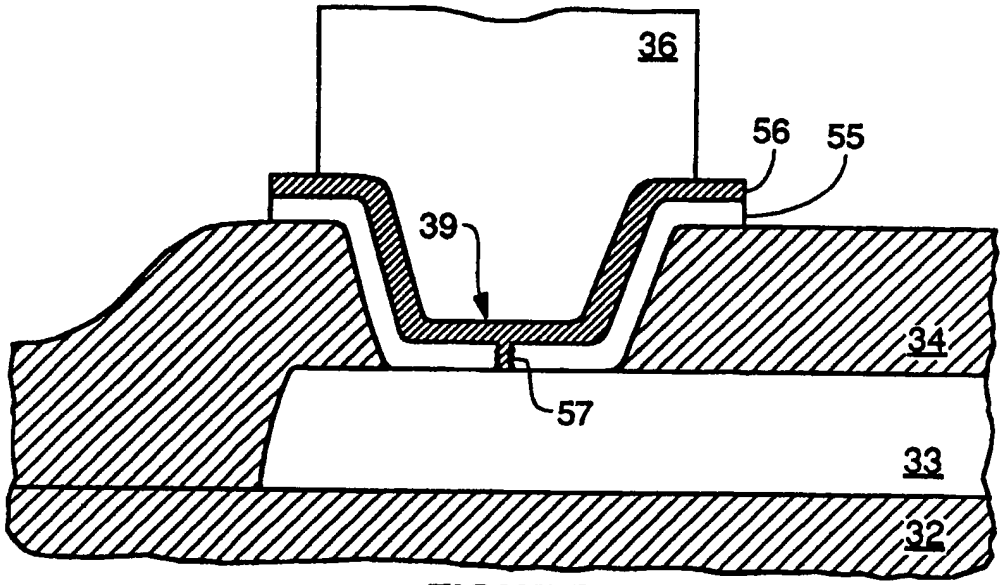


FIGURE 6

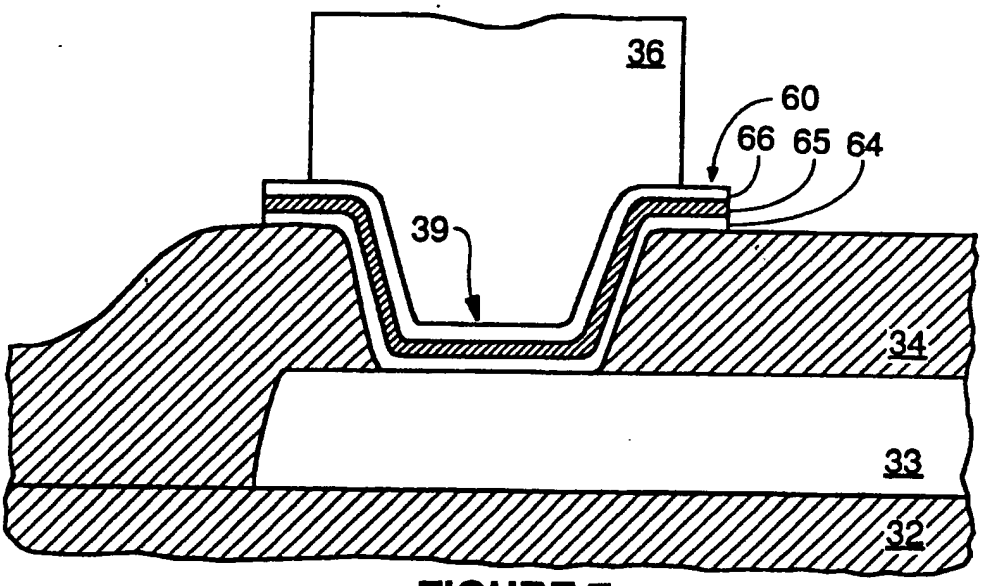
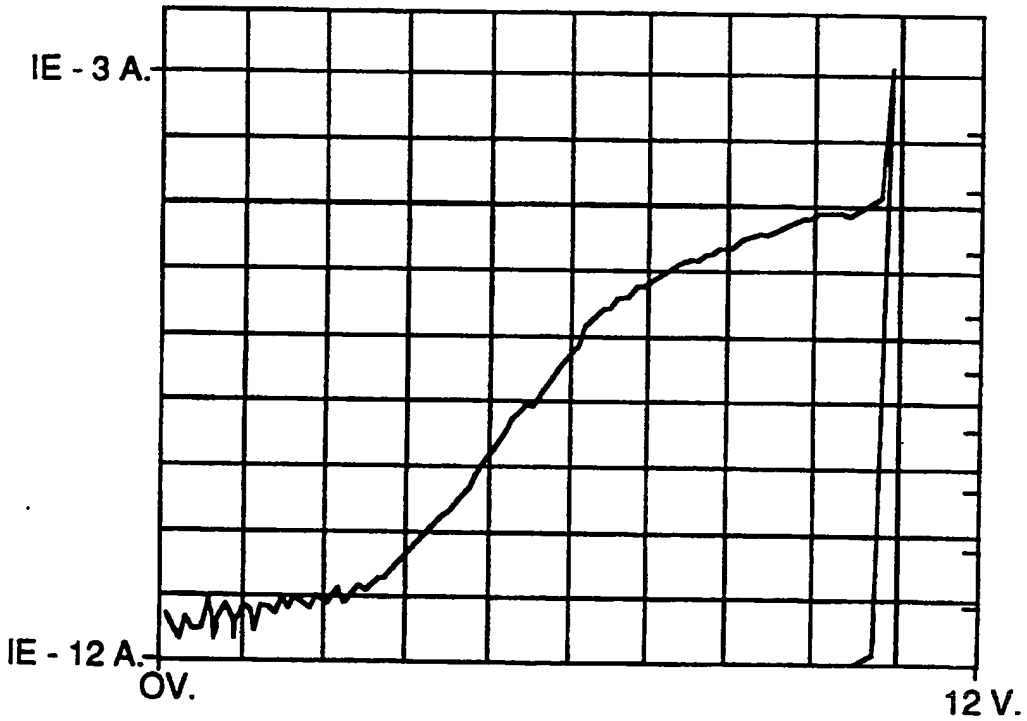


FIGURE 7

FIGURE 9



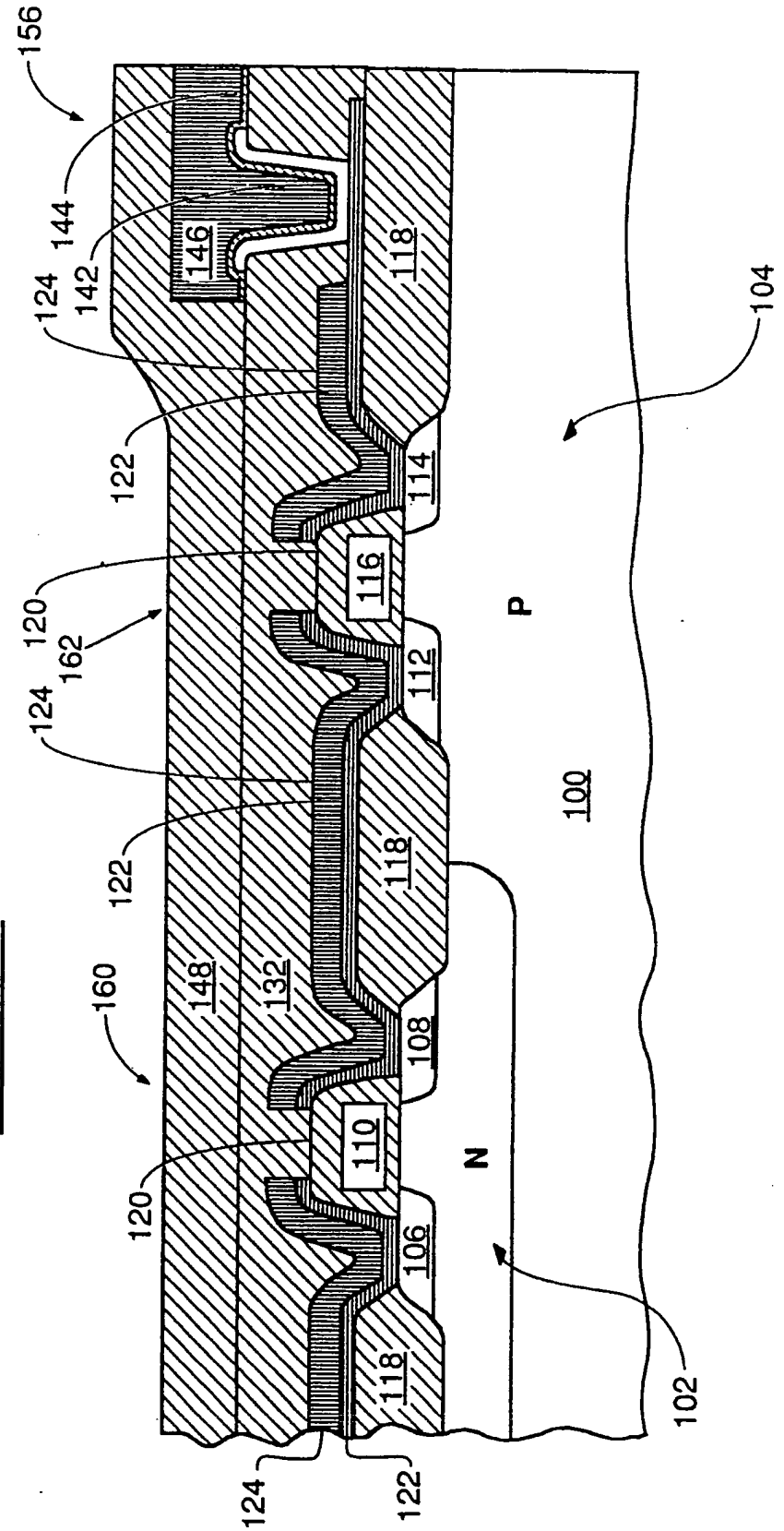
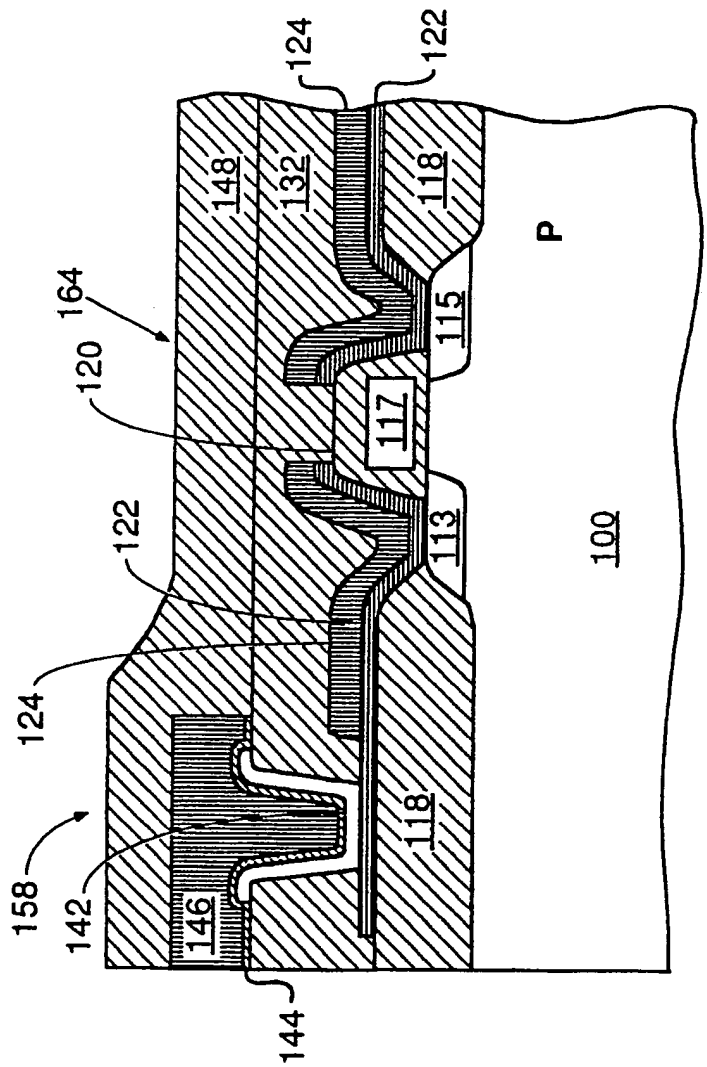

156
144
142
146
124
122
118
104
120
162
116
114
112
P
124
122
118
100
160
148
132
108
110
120
N
106
118
102
124
122

FIGURE 8A

FIGURE 8B


124
122
148
132
118
164
120
115
117
122
113
P
100
124
118
158
142
146
144